IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently amended) A method of improving yield in a multiple way associative cache memory having a plurality of cache blocks and a plurality of tag arrays each corresponding to one of the multiple ways, the method comprising:

determining whether a defect exists in any of the cache blocks;

for each way, storing, in a memory device separate from said tag arrays, a way select value indicative of whether the corresponding cache block is defective, and

for each way, selectively disabling the way if the corresponding cache block is defective by passing a match signal from each tag array through a select device, said select device forcing said match signal to indicate a mismatch condition in response to a corresponding one of said way select values.

2. (Canceled)

3. (Currently amended) The method of Claim 1, ~~further comprising~~ wherein:

when one or more of said cache blocks are disabled, operating the remaining, non-disabled cache blocks as a less-associative cache memory.

4. (Canceled)

5. (Currently amended) The method of Claim [[4]] 1, wherein ~~the~~ said ~~forcing step~~ selectively disabling further comprises:

comparing ~~the~~ a requested tag address with a tag ~~tags corresponding to the disabled cache block~~ stored in each said tag array;

generating, ~~for each cache block, a~~ said match signal ~~indicating~~ indicative of ~~the~~ results of ~~the~~ said comparing ~~step~~; and

gating ~~the~~ each said match signals with said corresponding way select ~~values~~ value to force the mismatch condition for comparison results ~~corresponding to the~~ of a disabled cache block.

6. (Currently amended) The method of Claim [[4]] 1, wherein during a cache write operation the disabling step comprises:

configuring a cache replacement algorithm to never select the disabled cache block.

7. (Currently amended) A method of improving yield in an N way associative cache memory having N cache blocks and N tag arrays corresponding to the N ways, the method comprising:

determining whether a defect exists in a cache block;

for each way, storing, in a memory device separate from said N tag arrays, a way select value indicative of whether the corresponding cache block is defective;

for each way, disabling ~~the cache block if there is a defect in the cache block~~ the way when a corresponding one of said way select values indicates a defective cache block by passing a match signal from each tag array through a select device, said select device selectively forcing said match signal to indicate a mismatch condition; and

operating ~~the~~ remaining cache blocks as an N-1 way associative cache memory.

8. (Canceled)

9. (Canceled)

10. (Currently amended) The method of Claim ~~9~~ 7, wherein ~~the~~ said ~~forcing step~~ disabling further comprises:

comparing a requested tag address with a tag ~~tags corresponding to the disabled cache block~~ stored in each said tag array;

generating ~~a~~ said match signal in response to ~~the~~ said comparing ~~step~~; and

gating the match signal with ~~a~~ said corresponding way select value to selectively force the mismatch condition.

11. (Currently amended) A multiple-way associative cache memory, comprising:

a plurality of cache blocks, each having a number of cache lines to store data;

a plurality of tag arrays, each storing a number of tags for associated data in a corresponding one of the plurality of cache blocks; and

select means ~~connected to both the cache blocks and the tag arrays,~~ receiving a match signal from each said tag array, said select means comprising a memory device separate from said tag arrays that stores a way select value for each said cache block, each said way select values being indicative of whether a corresponding one of said cache blocks is defective, the select means configured to selectively disable one or more of the ~~plurality of~~ cache blocks by forcing said match signal to indicate a mismatch condition for each tag array corresponding to cache blocks indicated by said way select value as being defective.

12. (Currently amended) The cache memory of Claim 11, wherein the select means further comprises: ~~a plurality of memory devices, each for storing a way select value for a corresponding cache block;~~ a plurality of gating circuits, each having a first input terminal coupled to receive said ~~a~~ match signal from a corresponding one of said tag arrays, a second input terminal coupled to receive a corresponding one of said ~~corresponding~~ way select values, and ~~having~~ an output terminal ~~to provide~~ thereby providing a gated match signal for a corresponding one of said cache blocks.

13. (Original) The cache memory of Claim 12, further comprising:

an encoder circuit having a plurality of input terminals coupled to receive the gated match signals for corresponding cache blocks, and having an output terminal to provide a select signal; and

a multiplexer having a plurality of input terminals coupled to receive data from corresponding cache blocks, an output terminal to provide output data, and a control terminal to receive the select signal.

14. (Original) The cache memory of Claim 13, wherein the select signal selects which cache block provides its data as the output data.

15. (Canceled)

16. (Currently amended) The cache memory of Claim ~~12~~ 11, wherein the memory devices comprises fuses.

17. (Original) The cache memory of Claim 12, wherein the gating circuits comprise AND gates.